

## **REMARKS**

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

### *Objections to the Specification*

The specification is objected to because of certain informalities. The specification has been amended to remove the identified informalities.

### *Objections to Drawings*

The drawings are objected for certain informalities. Applicants have submitted herewith the corrected drawing sheets.

### *Claim Objections*

Claims 1, 8, and 17 are objected to for containing certain informalities. Claims 1, 8, and 17 have been amended to remove the informalities.

### *Claim Rejections under 35 USC §102(e)*

Claims 1, 2, 8, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Publication No. 2003/0076839 (Li et al.). Applicants respectfully traverse these rejections.

To anticipate a claim, the reference must teach every element of the claim. *See* MPEP §2131. As to claim 1, Li et al. do not teach each and every element of claim 1.

Applicants respectfully point to the Examiner that claim 1 recites two distinct elements, a first direct access memory unit and a second direct access memory unit. In rejecting claim 1, the Examiner has cited Figure 1, reference 12 as the first direct memory access unit as recited in claim 1; however, the Examiner has cited the very same element, reference 12, as the second direct memory access unit as recited in claim 1. Li et al. do not show or describe reference 12 as a first and a second direct access memory unit and the Examiner has also not cited any reference in Li et al. as describing two distinct direct memory access units as recited in claim 1.

Further, as to the channel identification as recited in claim 1, the Examiner has stated that “...since there are multiple local memory units (Figure 1, references 140-14N) corresponding to multiple processing cores, then each local memory unit corresponds to a different channel in connection with the direct memory access unit as shown in Figure 1, hence each channel is separately identified (channel identification) so that the data can be passed to the correct processing core) ...” (emphasis added). However, as to the user-to-user identification as recited in claim 1, the Examiner has stated the same reasoning as the channel identification. For example, the Examiner has stated that “...since there are multiple local memory units (Figure 1, references 140-14N) corresponding to multiple processing cores (Figure 1, references 150-15N), then each local memory unit corresponds to a different channel in connection with the direct memory access unit as shown in Figure 1 (thus each channel having its own identification), and since each processing core (user) receives only the data meant for it (user indication), that data is not sent to the other processing cores (filtered)).” (Emphasis added).

Applicants respectfully point to the Examiner that first, Lie et al. do not describe any “memory channel identification” as the Examiner has stated; Second, claim 1 recites two distinct identifications; channel identification (CID) and user-to-user identification (UUI) where the Examiner has used the same reasoning as to the channel identification and user-to-user identification without any specific citation in Li et al. Therefore, Li et al. do not teach each and every element of claim 1. Accordingly claim 1 is patentably distinguishable from Li et al.

Claim 2 depends from claim 1 and is patentably distinguishable form Li et al. for at least the same reasons as claim 1.

As to claim 8, the Examiner has cited the same element, reference 12, three times for three different elements recited in claim 8 such as, a switching processor, a first direct memory access unit, and a second direct memory access unit. Applicants respectfully point to the Examiner that to anticipate a claim under 35 USC §102(e), a reference must teach each and every element of the claim. *See* MPEP §2131. The Examiner has not cited any reference that show, teach, or suggest a switching processor, a first direct memory access unit, and a second direct memory access unit as recited in claim 1. Therefore, Li et al. do not teach each and every element of claim 8 and accordingly, claim 8 is patentably distinguishable from the cited reference.

Claim 9 depends from claim 8 and is patentably distinguishable from Li et al. for at least the same reasons as claim 8.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



Abdul Zindani  
Attorney for Applicant  
Reg. No. 46,091

Texas Instruments Incorporated  
P.O. Box 655474, MS 3999  
Dallas, TX 75265  
(972) 917-5137